<u>Confirmation No. 7347</u>

<u>IN THE UNITED STATES PATENT AND TRADEMARK OFFICE</u>

Applicant:	SHRIVASTAVA, *et al.*	Examiner:	Knoll, C.
Serial No.:	10/566,515	Group Art Unit:	2111
Filed:	January 30, 2006	Docket No.:	US030254US2

Title: MICROCONTROLLER WITH AN INTERRUPT STRUCTURE HAVING PROGRAMMABLE PRIORITY LEVELS WITH EACH PRIORITY LEVEL ASSOCIATED WITH A DIFFERENT REGISTER SET

<u>**REPLY BRIEF UNDER 37 C.F.R. § 41.41**</u>

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Dear Sir:

This is a Reply Brief submitted pursuant to 37 C.F.R. § 41.41(a)(1) for the above-referenced patent application. In response to Appellant's Appeal Brief (dated May 20, 2008), the Examiner filed the Examiner's Answer (dated August 11, 2008). This Reply Brief is intended to supplement Appellant's Appeal Brief and all arguments therein are maintained unless expressly stated otherwise.

Appellant believes that no fee is due. However, authorization to charge/credit **Deposit Account number 50-0996 (NXPS.281PA)** is hereby given in case there are additional fees/overages in support of this filing.

Status of Claims

Claims 1-21 stand rejected and are presented for appeal.

Grounds of Rejection to be Reviewed Upon Appeal

A.   Claims 1-7, 11, 13-16 and 19-21 stand rejected under 35 U.S.C. § 103(a) over Mitsuhira (U.S. Patent No. 5,155,583) in view of Yoshida (U.S. Patent No. 5,450,566).

B.   Claims 8-10 and 17-18 stand rejected under 35 U.S.C. § 103(a) over Mitsuhira (U.S. Patent No. 5,155,583) in view of standard register use, and in further view of Fujimura (U.S. Patent No. 5,751,988).

C.   Claim 12 stands rejected under 35 U.S.C. § 103(a) over Mitsuhira (U.S. Patent No. 5,155,583) in view of standard register use, and in further view of Hohl (U.S. Patent No. 6,035,422).

Argument

The following discussion is presented both as a response to specific arguments presented in the Examiner's Answer and as further support for Appellant's positions stated in the underlying Appeal Brief (which fully addresses each of the issues raised in the Examiner's Answer even in the absence of this Reply Brief). In this Reply Brief, Appellant addresses three issues. The first issue is common among each of the Examiner's responses, and relates to the Examiner's unreasonable and unsupported definition of the phrase "special function register." The second and third issues rebut specific mischaracterizations by the Examiner, which relate to the misinterpretation of "special function registers."

Appellant requests that the following discussion be considered by the Board in conjunction with Appellant's Brief to reach a favorable decision.

Issue 1: The Examiner's definition of "special function register" is unreasonable and unsupported, and further is inconsistent with the record including Appellant's Specification, the cited art, and materials cited by Appellant.

The Examiner tacitly admits that the rejections would fail for lack of foundation upon rejecting the Examiner's proffered definition of "special function registers" in favor of Appellant's explanation. Appellant therefore submits that one main issue involves the choice between the Examiner's unsupported interpretation, and Appellant's explanation, which is consistent with the usage of "special function registers" throughout the record, including in Appellant's Specification, the cited references, and additional supporting material cited by Appellant.

Appellant submits that special function registers are understood to those of skill in the art to store information in a processor for access as internal memory, the stored information being specific to controlling the various functions of the processor. This is consistent with Appellant's claims and specification, the cited Mitsuhira reference, and is evidenced by cited U.S. Patent No. 5,734,857 and the printout provided by Appellant from http://www.hobbyprojects.com/8051_tutorial/special_function_registers.html. each of which were presented in the Appeal Brief and the Response of September 7, 2007. As explained in connection with cited U.S. No. 5,734,857, the skilled artisan is familiar with

Intel's microprocessors and the Intel 8051 best exemplifies the skilled artisan's understanding of the term being consistent with Applicant's position. U.S. No. 5,734,857 defines this term as follows: "Many microprocessors, notably those based on the type 8051, comprise a number of registers which <u>are referred to as special-function registers</u> and which can be directly addressed in a particularly simple manner by means of given instructions." See No. 5,734,857, Col. 2, lines 25-29 (emphasis added).

As explained at Section 2111.01(III) of the M.P.E.P., "The ordinary and customary meaning of a term may be evidenced by a variety of sources, including 'the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. *Phillips v. AWH Corp.*, 415 F.3d at 1314, 75 USPQ2d at 1327." For the claim term "special function register", Appellant has submitted a variety of sources, including all of the above-mentioned sources. The words of the claims themselves are used in the same word-for-word manner as used in the remainder of the specification, above-noted references (*e.g.*, re: the Intel 8051 processor) in the prosecution history, and the state of the art evidencing accepted use of Appellant's interpretation of this claim term (*e.g.*, as emanating from widespread use of the Intel 8051 processor and other processor). In contrast, the Examiner has not presented any evidence of any use of the term "special function register". Rather, in violation of M.P.E.P. 2111.01(III), the Examiner attempts to disregard the evidence in support of, and the rules for assessing whether this term is carried by, Appellant's interpretation.

Accordingly, the uncontroverted record establishes that the claim term "special function register" has an ordinary and customary meaning that further distinguishes Appellant's claimed invention, as the asserted prior art teaching does not have a "special function register" which, in its ordinary and customary meaning, is directed to a processor-internal register for specific processor functions such as Appellant's claimed logic and arithmetic processor operations. *See, e.g.*, Appellant's claim 1.

The data memory 36 disclosed by Mitsuhira, and alleged by the Examiner to constitute special function registers, is a memory location external from the processor (CPU 16) which is used to temporarily store a copy of certain data from the CPU 16. The

temporarily stored data is then restored to the CPU 16 rather than accessed as internal memory. *See, e.g.*, Mitsuhira Col. 4:45-62. Appellant submits that Mitsuhira's teachings are consistent with the registers of data memory 36 being used as "general registers," and indeed are called general registers by Mitsuhira. *See, e.g.*, Mitsuhira Col. 4:45-62. Whether or not the registers of data memory 36 may be used for processor-related functions does not make them "special function registers" because they are not stored in the processor for access as internal memory. In other words, it is not merely the use of a register that makes it a "special function register," as the Examiner would have the Board believe.

In parsing the Examiner's interpretation, it appears that the Examiner considers a "special function register" to be any memory that can be used in the performance of a function, such as an arithmetic function, in a manner that the Examiner has subjectively decided is special, for example as an interrupt (*see, e.g.*, Examiner's Answer page 8). Appellant observes that such a broad interpretation, drawn in an attempt to encompass Mitsuhira's data memory 36, appears to describe virtually any register. The Examiner's interpretation thus voids any meaning and distinction from terms such as "special function register" and "general register," and therefore is unreasonable.

Appellant submits that, faced with choosing between the meanings of "special function register" ascribed by Appellant's Specification and consistent with the totality of the record, and the Examiner's overly-broad interpretation that appears to be subjective and lacks any evidentiary support, the Board's choice is clear.

Issue 2: The Examiner's citation to an accumulator (ACC) in Appellant's submission as an example of a special function register is supportive of Appellant's arguments, not the Examiner's.

In arguing that it is known for special function registers to perform arithmetic functions, the Examiner's Answer cites to the ACC register discussed in Appellant's submitted web page printout (referenced above). *See* Examiner's Answer, page 10. Again, the Examiner focuses solely on the function and use of the register, and ignores the fact that the ACC register is used internally by the processor, and is accessed as internal memory. As discussed, Mitsuhira's data memory 36, alleged by the Examiner to constitute special

function registers, does not share these characteristics, and therefore cannot be equated to the ACC registers from Appellant's submission.

Issue 3: The Examiner mischaracterizes Appellant's arguments regarding an object of the present invention.

In the Appeal Brief, Appellant observed that an object of certain embodiments of Appellant's invention is to facilitate the execution of an interrupting program stream without storing and restoring interrupted program stream critical data (*see, e.g.,* Appellant's Specification, Paragraph 0005). Appellant further observed that Mitsuhira teaches storing and restoring critical data in response to interrupt requests. Such observations were meant to further illustrate why Mitsuhira's data memory registers cannot be considered special function registers.

The Examiner's Answer appears to misinterpret Appellant's argument as a statement that the claims are limited to facilitating the execution of an interrupting program stream without storing and restoring interrupted program stream critical data. In accordance with the observations above, this is clearly not the case.

Conclusion

In view of the above, Appellant submits that the rejections of claims 1-21 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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Respectfully Submitted,

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